STM32MP1 System-On-Module (SOM)

Hardware Architecture

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1. Introduction

This document describes the hardware architecture of the Emcraft Systems ST32MP1 System-on-Module (referred to as “STM32MP1 SOM” hereafter).

The STM32MP1 SOM is intended to provide a low-cost flexible platform for embedded solutions that require rich connectivity and flexibility of the ST32MP157 microprocessor device. The STM32MP1 SOM is based on the ST ST32MP157 dual-core, versatile, low-power, high-integration microprocessor. The Linux kernel and applications execute on the ARM Cortex-A7 650MHz processor core, while an RTOS runs on the ARM Cortex-M4 209MHz processor core. The integrated peripheral controllers of the ST32MP157 are used to implement various communication, connectivity and human-machine interfaces.

Using a miniature mezzanine form factor, the STM32MP1 SOM is specifically designed to provide the primary ST32MP157 intelligence on various boards targeting industrial automation, system and power management, wired and wireless networking / sensors and other embedded applications. The STM32MP1 SOM is architected as a low-cost solution with flexibility in customizing its functionality for the needs of particular products and customers.

2. Hardware Platform

This section defines the hardware platform of the STM32MP1 SOM.

2.1. Hardware Platform Overview

The following are the key hardware features of the STM32MP1 SOM:

- Compact mezzanine module (32mm x 59mm);
- External interfaces using two 100-pin 0.4mm-pitch connectors;
- Two mounting holes reducing the risk of connector-to-PCB intermittence;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- ST ST32MP157 dual-core microprocessor with the ARM Cortex-A7 (up to 650MHz) and Cortex-M4 cores (up to 209MHz);
- JTAG interface to the ST32MP157;
- Powered from a single +3.3V power supply;
- Low-power operational modes with fast wake-up;
- On-module clocks;
- 1024MBytes DDR3L SDRAM;
- 4GB eMMC storage;
- Serial console interface at the UART CMOS levels;
- 1Gb Ethernet interface with on-module PHY;
- MIPI DSI 2 data lanes up to 1GHz each;
- Two high speed (HS) USB 2.0 (up to 480Mbps), with integrated HS USB PHY (1xUSB 2.0 with OTG support);
- TFT LCD interface;
- Various serial digital (UART, SPI, I2C, SDHC, SAI) and analog interfaces of the ST32MP157 available on the interface connectors.

2.2. Functional Block Diagram

The following figure is a functional block diagram of the STM32MP1 SOM:

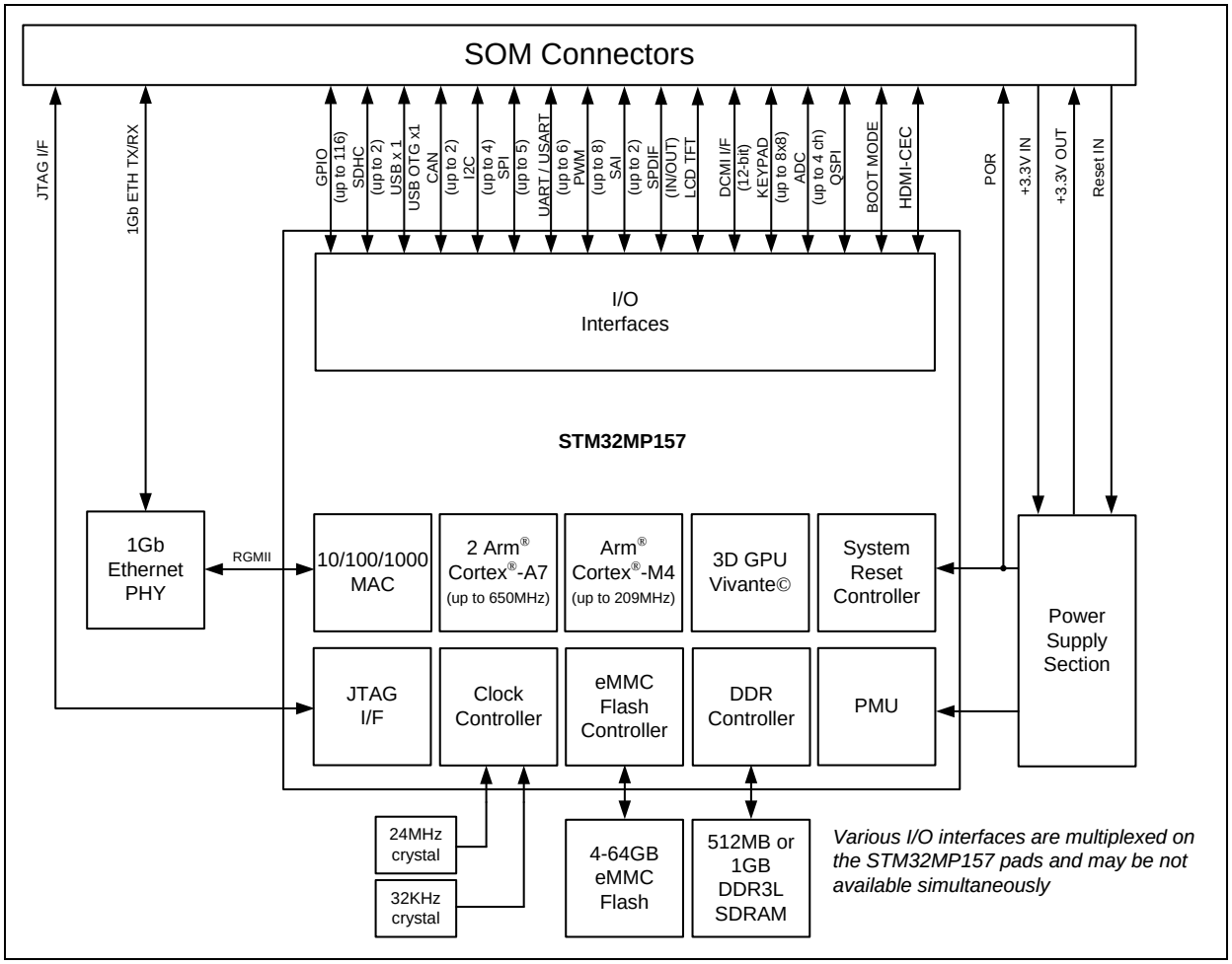

Figure 1: STM32MP1 SOM Functional Block Diagram

2.3. Microcontroller

2.3.1. Microcontroller Device

The architecture of the STM32MP1 SOM is built around the ST ST32MP157 dual-core microcontroller that combines the ARM Cortex-A7 (up to 650MHz) and Cortex-M4 (up to 209MHz) processor cores with a wide range of the integrated peripheral controllers.

The ST32MP157 device is implemented using the 18mm x 18mm 0.8mm-pitch Map BGA package.

2.3.2. Microcontroller Configuration

The STM32MP1 SOM supports the following ST32MP157 devices (SOM build-time options):

- STM32MP1 57CAA;
- STM32MP1 57AAA.

2.3.3. Microcontroller Boot Selection

The ST32MP157 ROM code is configured to use the on-module eMMC memory as a boot device. This is achieved by using the boot-mode resistors installed on the ST32MP157 pin BOOT0, BOOT1 and BOOT2.

Please refer to the *ST32MP157 RM0436 Reference manual* for the boot selection description.

Note that the above boot pins are also routed to the SOM connectors P1 and P2 (refer to Section 2.13.2). Care must be taken not to override the state of the above pins during boot time on a carrier board, otherwise the STM32MP1 SOM may fail to boot.

2.4. JTAG Interface

The STM32MP1 SOM provides a standard JTAG interface on the interface connectors. This interface is routed to the corresponding signals of the ST32MP157 device.

2.5. Power

2.5.1. Power Source

The ST32MP157 is run from a single +3.3V power source provided through multiple pins on the interface connectors.

2.5.2. Power Modes

The STM32MP1 SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation. The main clock is running and the Cortex-A7 and Cortex-M4 cores are running Linux and RTOS, respectively. All memory controllers are enabled.

  Software is configured to enable only those ST32MP157 sub-systems that are used by installed device drivers; the clocks to all other sub-systems are gated off so those modules do not consume power.

- Low-power mode. This is Linux low-power mode, also referred to as the “Linux suspend-to-ram” mode of operation. When Linux is commanded to enter the low-power mode, it transitions the SDRAM device to the self-refresh mode, ensuring that the Linux operational content is preserved across the low-power mode. The on-module Ethernet PHY is put into a low-power mode. The Cortex-A7 and Cortex-M4 cores are put into appropriate low power modes.

  To put external (on-carrier) devices into low-power mode, the STM32MP1 SOM provides a dedicated output signal as a control for switching off-module (on carrier) devices to low-power modes, as appropriate. This active-low signal is implemented using a GPIO of the ST32MP127 device and is available as SUB_NRST(PD10) on the interface connectors. When switching the system to the low-power mode, software activates the low-power mode signal. Off-module devices are expected to react to activation of that signal by switching themselves to low-power modes, as appropriate for the carrier design. Conversely, when software is switching back to full-power mode, it de-asserts the low-power mode signal indicating to off-module devices that they are expected to switch back to the full-power mode.

  The STM32MP1 SOM remains in the low-power mode until woken up by a configured trigger (such as, for instance, activation of a configured GPIO). On occurrence of a wake-up trigger, the STM32MP1 SOM returns to the full-power mode.

2.6. System Reset

2.6.1. Reset Architecture Overview

The STM32MP1 SOM implements a reset architecture that ensures that the ST32MP157 microprocessor is reset as appropriate on various hardware and software events.

The STM32MP1 SOM ensures that the on-module Ethernet PHY is reset as soon as the ST32MP157 device is subjected to reset. This is achieved by connecting the reset signal ETH_NRST (PD11) to the reset inputs of the Ethernet PHY device.

Those off-module devices that require synchronizing their resets with STM32MP1 SOM resets must connect the active-low SUB_NRST signal to the reset input of a respective off-module device.

2.6.2. Types of System Resets

The following types of reset are implemented by the STM32MP1 SOM:

- Power-on reset. This type of reset occurs when the power is initially applied to the STMP1STMP1-SOM. As the supply voltage rises, the on-SOM Low-Voltage Detect (LVD) system holds the ST32MP157 in reset until all the processor power supply voltages have risen above the appropriate voltage thresholds (+3.075V, typical, for the +3.3V power rail). The internal ST32MP157 power-on reset generation is disabled.
- Brown-out reset. In case any processor supply falls below its lower voltage threshold, the LVD system generates a reset of the ST32MP157. After the brown-out reset has occurred, the LVD system holds the ST32MP157 in reset until all the supplies have risen above their upper thresholds .

The aforementioned resets are implemented by using the STM32MP1 57 NRST signal/pin. This signal is named NRST on the SOM connector and intended for using by the JTAG programmer only. This signal mustn't be driven by any other user device. For embedded designs that may be subject to excessive noise in the vicinity of the nPOR net, it is recommended to add a 100-3000pF capacitor to the nPOR net on a carrier board.

- Software reset. This type of reset is activated by software running on the STM32MP1 SOM through performing the ST32MP157 software reset sequence.
- WDT reset. This type of reset is activated when the integrated ST32MP157 WDG expires.
- External reset. To activate this type of reset, a baseboard drives low the nMR signal on the STM32MP1 SOM interface connectors.

2.7. System Clocks

The STM32MP1 SOM provides a 24MHz quartz crystal as a reference to the internal oscillator of the ST32MP157 microprocessor.

2.8. SDRAM

2.8.1. SDRAM Architecture

The STM32MP1 SOM provides 1024MBytes of DDR3 SDRAM using the following device:

- Micron MT41K256M16TW-107:P

The DDR3 resides at the DDR_CSN chip select of the integrated SDRAM controller of the ST32MP157 device.

2.8.2. SDRAM Operational Mode

The ST32MP157 SDRAM controller operates in the DDR3L Mode. The DDR clock frequency of the SDRAM controller is 533MHz.

2.9. EMMC

2.9.1. EMMC Architecture

The STM32MP1 SOM provides 4GBytes of eMMC memory using the Kingston EMMC04G-M627-X02U EMMC device. The eMMC memory resides at the SDMMC2 interface of the ST32MP157 integrated eMMC controller.

2.10. Serial

2.10.1. Serial Console Interfaces

The STM32MP1 SOM provides UART serial interfaces at CMOS levels (no RS-232 buffers) using the integrated USART1 and UART4 controllers of the ST32MP157 MCU on the interface connector.

2.10.2. Serial Baud Rate

The UART controllers feature an internal divider that allows these serial interfaces to operate at standard baud rates up to 12.5Mbit/s. The default firmware setting is 115200 bod.

2.11. Ethernet

2.11.1. Ethernet Controllers

The STM32MP1 SOM provides one Ethernet interface:

- 1Gb Ethernet interface buffered by the on-module 1Gb Ethernet PHY device.

2.11.2. Ethernet Physical Layer

The physical layer of the 1Gb Ethernet interface is implemented using the Qualcomm AR8031-AL1A Ethernet PHY device to provide the full-featured 10/100/1000Mbps IEEE 802.3 interface.

2.11.3. Ethernet Clock

The STM32MP1 SOM uses an internal PLL of the ST32MP157 MCU for generation of the 25MHz clock for the on-SOM Ethernet PHY device. The RGMII reference clock is generated by the Gigabit Ethernet PHY and is provided to the ST32MP157 MAC.

2.11.4. Ethernet Status LEDs

The STM32MP1 SOM provides three status signals of the Ethernet interface on the interface connectors for controlling off-module Ethernet LEDs. The functionality of these signals is as follows:

- LED_ACT, used to indicate link status (Link when high, No Link when low) and the RX activity when toggling;
- LED_10/100, used to indicate the 10/100Mbit link status (100Mbit when low, 10Mbit when high);
- LED_1000, used to indicate the used to indicate the 1000Mbit link status, active low.

2.12. Watchdog

The ST32MP157 provides a hardware watchdog function using the integrated independent watchdogs (IWDG1 and IWDG2) dedicated to MPU and window watchdog (WWDG1) dedicated to the MCU of the ST32MP157.

Both watchdog peripherals (Independent and Window) allow detecting and resolving malfunctions due to software or hardware failures.

The IWDG1 and IWDG2 are dedicated to MPU, while the WWDG1 is dedicated to MCU. In addition, the IWDG1 is located onto a secure bus (APB5), and can only be accessed by a secure application when TrustZone is enabled.

All watchdogs are disabled by default after the reset. Software should enable or leave them disabled, as appropriate.

If software enables a WDOG and then fails to refresh it within the predefined period of time, the watchdog resets the corresponding module of the ST32MP157.

The watchdog timeout period is defined by software.

2.13. External Interface

2.13.1. Interface Connectors

The external interfaces of the STM32MP1 SOM are routed through two 100-pin Hirose DF40 series 0.4mm-pitch board-to-board connectors.

2.13.2. Connectors Pin-Out

Refer to the stm32mp1-som-pinout.xlsx file available from the Emcraft web site for the detailed information on connectors pin-out.

3. Mechanical Specifications

3.1. STM32MP1 SOM Mechanicals

The STM32MP1 SOM is implemented as a miniature 32mm x 59mm x 5.4mm module.

The STM32MP1 SOM PCB thickness is 1.6+/- 0.16mm. The maximum height of the SOM components on the both sides of the module is 1.mm.

The STM32MP1 SOM includes two mounting holes so that the module can be mechanically secured to a baseboard, reducing the risk of connector-to-PCB intermittence that might occur during NEBS vibration and earthquake testing (or during real events that those tests simulate).

The following figure shows the location of the mounting holes and the SOM connectors on the module:

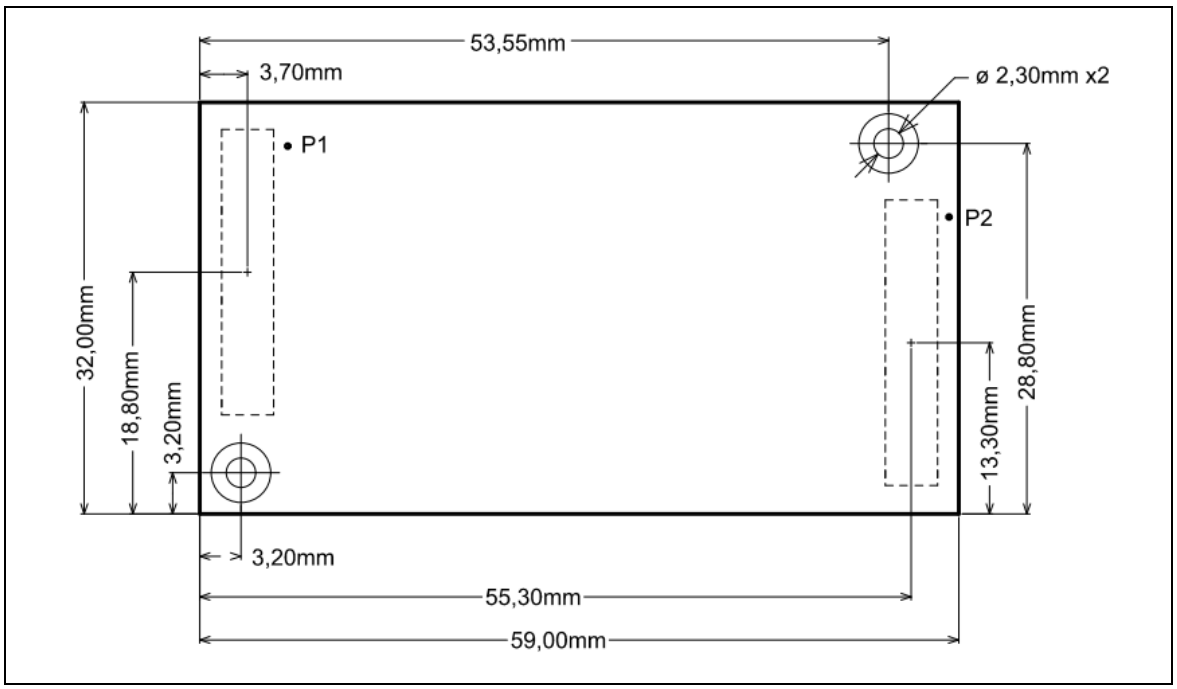

Figure 2: STM32MP1 SOM Top View

3.2. STM32MP1 SOM Connectors Mechanicals

On a baseboard, the STM32MP1 SOM is installed into two 100-pin Hirose DF40 series 0.4mm-pitch board-to-board connectors. The exact part number of the connectors is Hirose DF40C-100DP-0.4V. Mechanical details of the connectors can be found in the corresponding datasheet.

The recommended mating connectors for a baseboard is the Hirose DF40C-100DP-0.4V connector, which provides 3mm stacking height for the STM32MP1 SOM. The maximum height of the SOM above a baseboard for 3mm stacking height is 6.4mm.

3.3. STM32MP1 SOM Top and Bottom Views

The following pictures provide the top and bottom views of the STM32MP1 SOM:

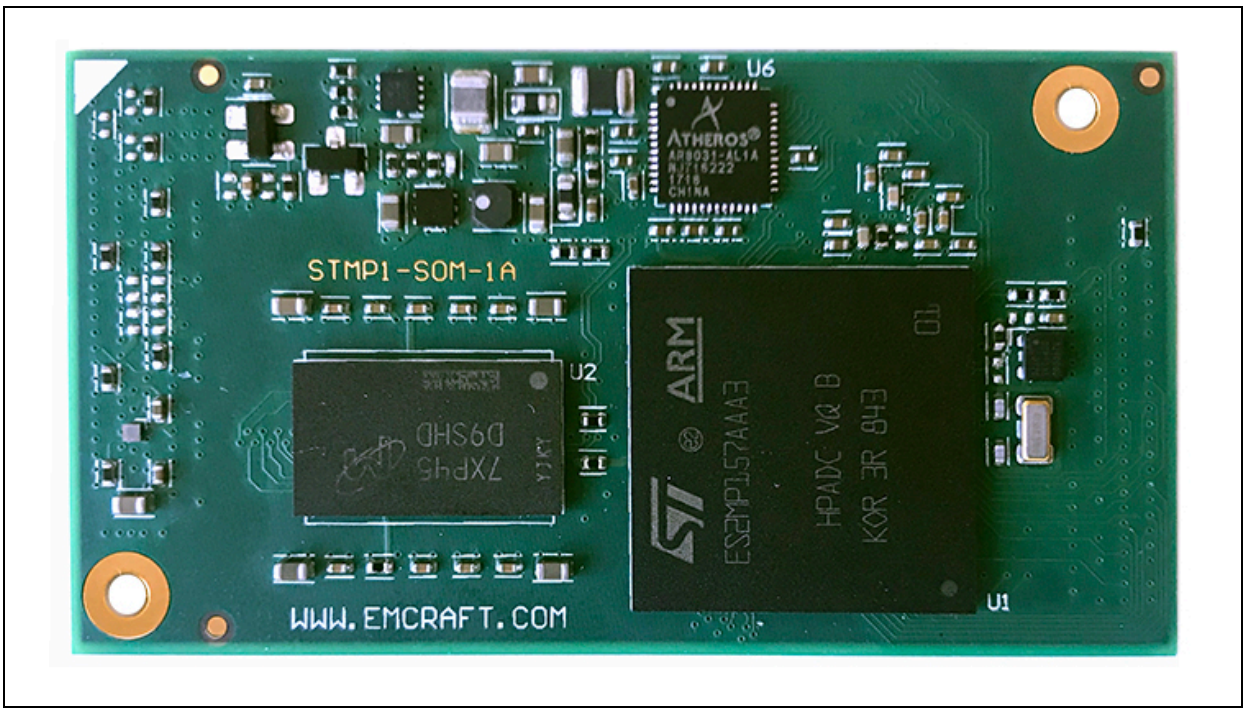

Figure 3: STM32MP1 SOM Top View

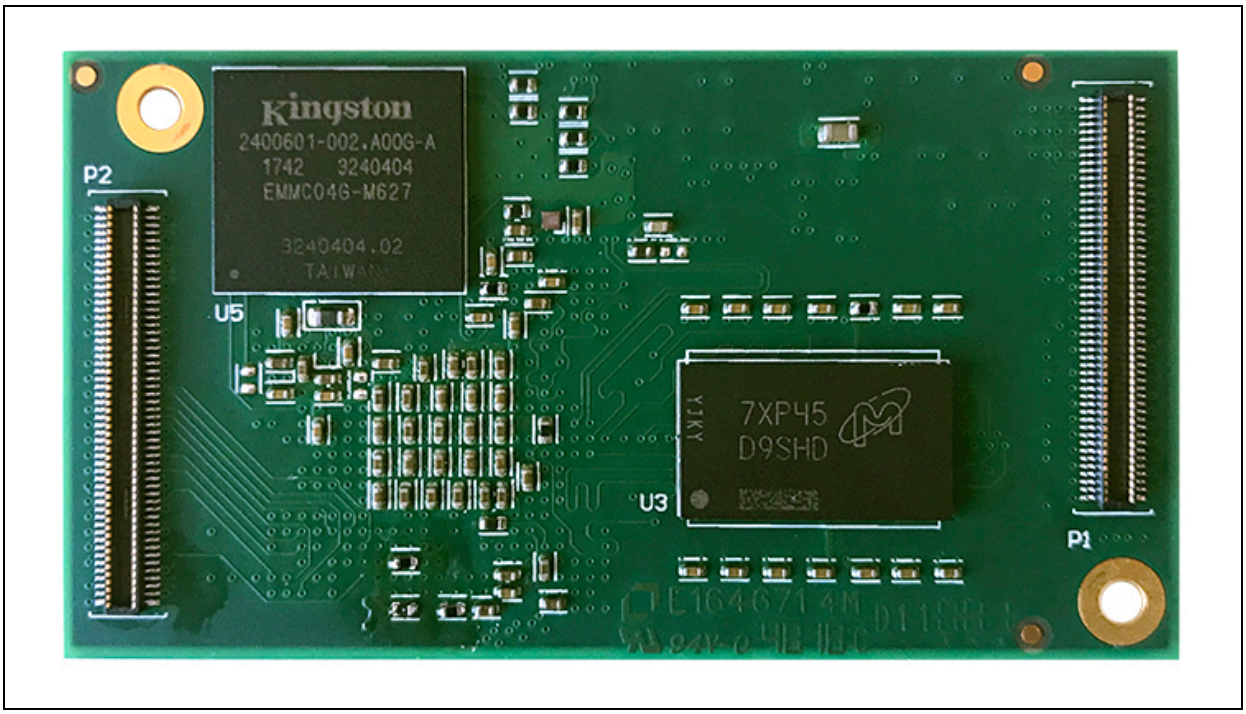

Figure 4: STM32MP1 SOM Bottom View

4. Environment Specifications

4.1. Recommended Operating Conditions

The following table lists the recommended operating conditions of the STM32MP1 SOM:

Symbol	Parameter	Range	
T_A	Ambient temperature	Commercial	0 to +70 ºC
VCC_IN	+3.3V power supply	+3.3V +/-5%	

Table 1: Recommended Operating Conditions

5. Ordering Specifications

The following table provides the ordering information for the STM32MP1 SOM:

Ordering Part Number	Specification
SOM-STM32MP1	ST32MP157, 650MHz Cortex-A7, 209MHz Cortex-M4, Commercial (0 to +70C), 1024MB RAM, 4GB eMMC, 1Gb ETH PHY

Table 2: Ordering Specification

6. Document Revision History

Revision	Date	Changes Summary
1.0	February 15, 2019	Initial version